Features

- Supply Voltage up to 40V
- Operating Voltage V_S = 5V to 18V
- Typically 10 µA Supply Current During Sleep Mode
- Typically 40 µA Supply Current in Silent Mode
- Linear Low-drop Voltage Regulator:
  - Normal Mode: V_{CC} = 5V ±2%/50 mA
  - Silent Mode: V_{CC} = 5V ±7%/50 mA
  - Sleep Mode: V_{CC} is Switched Off
- V_{CC} Undervoltage Detection with Reset Output NRES (10 ms Reset Time)
- Voltage Regulator is Short-circuit and Over-temperature Protected
- LIN Physical Layer According to LIN Specification Revision 2.0
- Wake-up Capability via LIN Bus (90 µs Dominant)
- TXD Time-out Timer (9 ms)
- 60V Load-dump Protection at LIN Pin
- Bus Pin is Overtemperature and Short-circuit Protected versus GND and Battery
- High EMC Level
- 5V CMOS-compatible I/O Pins to MCU
- ESD HBM 6 kV at Pins LIN and VS
- Interference and Damage Protection According to ISO/CD7637
- Package: SO8

LIN Bus Transceiver with Integrated Voltage Regulator

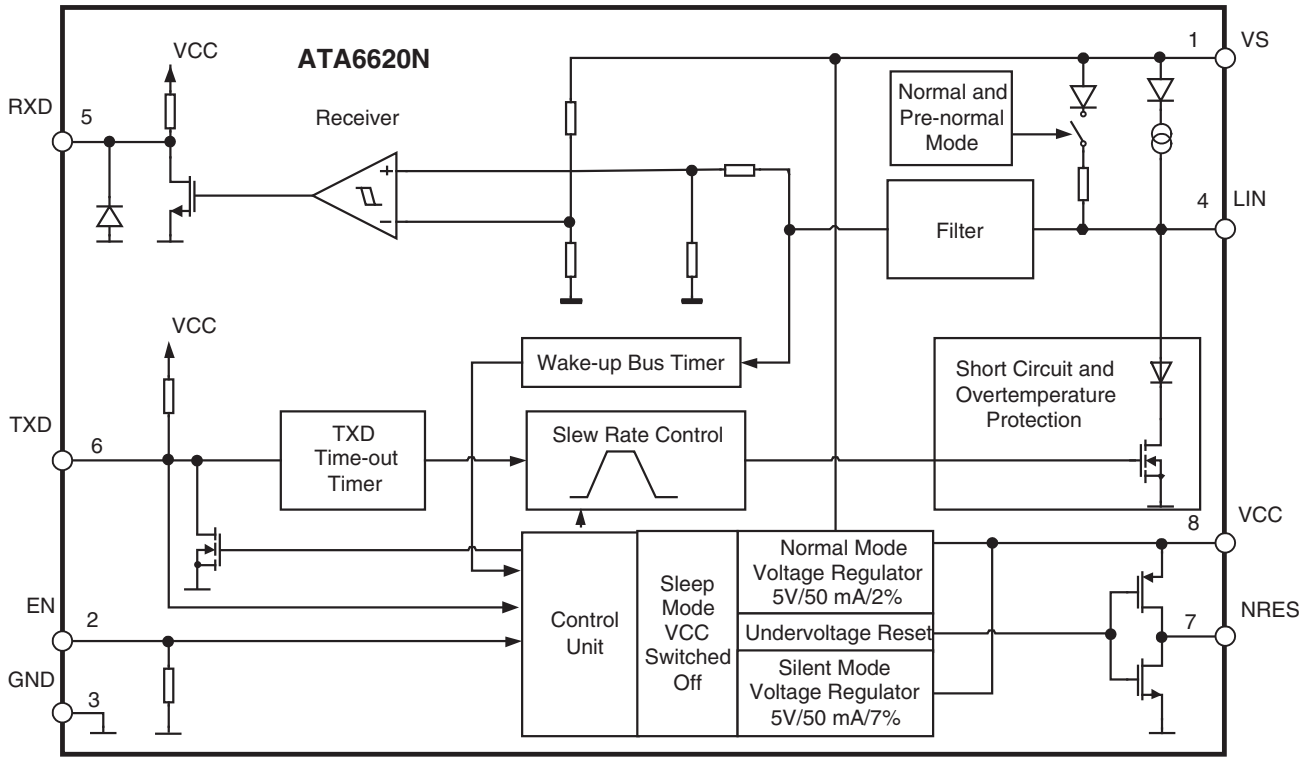
ATA6620N

1. Description

ATA6620N is a fully integrated LIN transceiver, designed according to the LIN specification 2.0, with a low-drop voltage regulator (5V/50 mA). The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful, slave nodes in LIN Bus systems. ATA6620N is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud with an RC oscillator for the protocol handling. The bus output is designed to withstand high voltage. Sleep mode (voltage regulator switched off) and Silent mode (communication off; V_{CC} voltage on) guarantee minimized current consumption.

4850I–AUTO–09/09

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO8

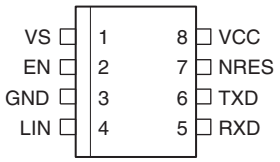


Table 2-1. Pin Description

Pin	Symbol	Function
1	VS	Battery supply
2	EN	Enables Normal mode if the input is high
3	GND	Ground
4	LIN	LIN bus line input/output
5	RXD	Receive data output
6	TXD	Transmit data input, active low output
7	NRES	Output undervoltage reset, low at reset
8	VCC	Output voltage regulator 5V/50 mA

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.0 can be mixed with LIN physical layer nodes, which, according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3), are without any restrictions.

3.2 Supply Pin (VS)

LIN operating voltage is V_S = 5V to 18V. After switching on V_S, the IC starts with the Pre-normal mode and the voltage regulator is switched on (that is, 5V/50 mA output capability).

The supply current in Sleep mode is typically 10 µA and 40 µA in Silent mode.

3.3 Ground Pin (GND)

The IC is neutral on the LIN pin in case of GND disconnection. It is able to handle a ground shift up to 3V for supply voltage above 9V at the VS pin.

3.4 Voltage Regulator Output Pin (VCC)

The internal 5V voltage regulator is capable of driving loads with up to 50 mA, supplying the microcontroller and other ICs on the PCB. It is protected against overload by means of current limitation and overtemperature shut-down. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold V_{thun}.

3.5 Undervoltage Reset Output (NRES)

This push-pull output is supplied from the V_{CC} voltage. If the V_{CC} voltage falls below the undervoltage detection threshold of V_{thun}, NRES switches to low after tres_f (see Figure 4-7 on page 11) except the IC is switched into Sleep mode. Even if V_{CC} = 0V the NRES stays low, because it is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays low until V_S < 1.5V and then becomes highly resistive.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 10 ms after V_{CC} reaches its nominal value.

3.6 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown, as well as an internal pull-up resistor according to LIN specification 2.0 is implemented. The voltage range is from –40V to +60V. This pin exhibits no reverse current from the LIN bus to V_S, even in the case of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification.

The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled. The output has a short-circuit limitation. This is a self-adapting current limitation; that is, during current limitation, as the chip temperature increases, the current decreases.

3.7 Input/Output Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state.

3.8 Dominant Time-out Function (TXD)

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 4 ms, the LIN bus driver is switched to the recessive state. To reset this dominant time-out mode, TXD must be switched to high (> 10 µs) before normal data transmission can be started.

3.9 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up structure with typically 5 kΩ to V_{CC}. The AC characteristics are measured with an external load capacitor of 20 pF.

The output is short-circuit protected. In unpowered mode (that is, V_S = 0V), RXD is switched off.

3.10 Enable Input Pin (EN)

This pin controls the operation mode of the interface. After power up of V_S (battery), the IC switches to Pre-normal mode, even if EN is low or unconnected (internal pull-down resistor). If EN is high, the interface is in Normal mode.

A falling edge at EN while TXD is still high forces the device to Silent mode. A falling edge at EN while TXD is low forces the device to Sleep mode.

4. Mode of Operation

Figure 4-1. Mode of Operation

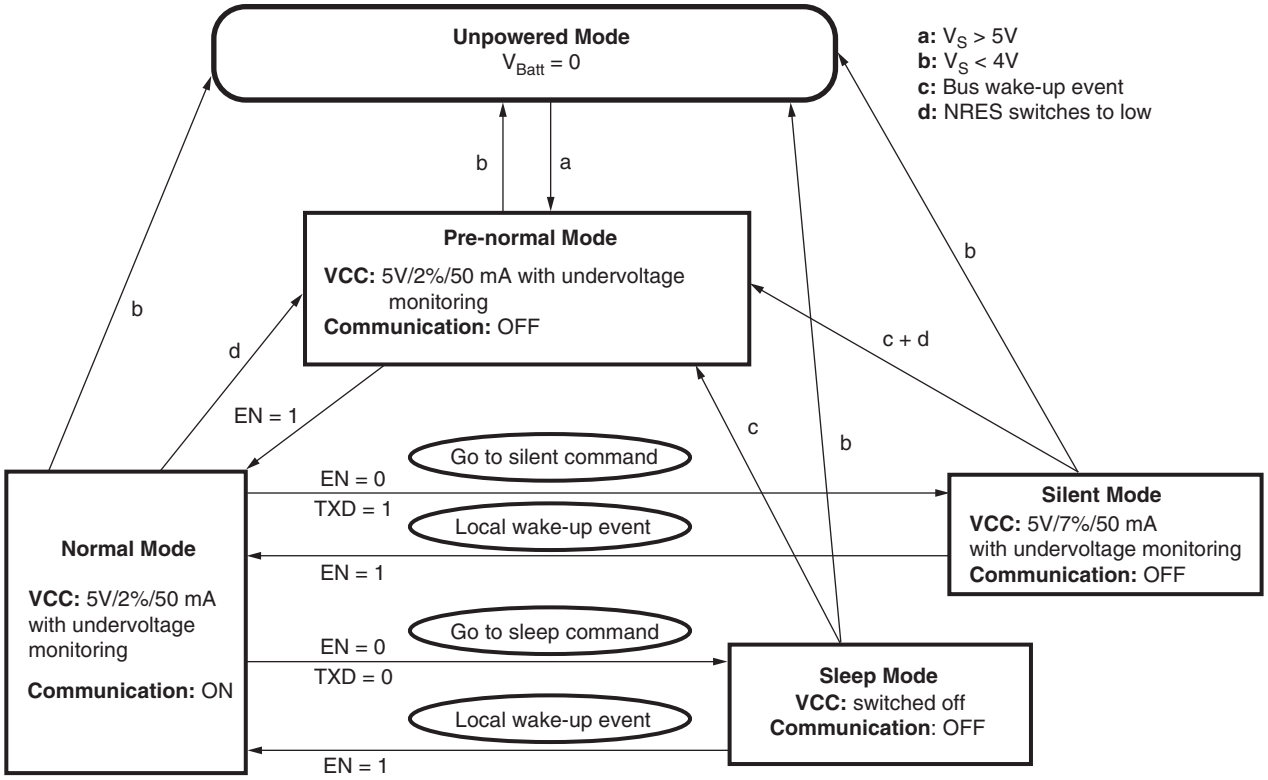


Table 4-1. Mode of Operation

Mode of Operation	Communication	V_{CC}	RXD	LIN
Pre-normal	OFF	5V	5V	Recessive
Normal	ON	5V	5V	Recessive
Silent	OFF	5V	5V	Recessive
Sleep	OFF	0V	0V	Recessive

4.1 Normal Mode

This is the normal transmitting and receiving mode of the LIN Interface, in accordance with LIN specification 2.0. The V_{CC} voltage regulator operates with a 5V output voltage, with a low tolerance of ±2% and a maximum output current of 50 mA.

If an undervoltage condition occurs, NRES is switched to low and the ATA6620N changes state to Pre-normal mode. All features are available.

4.2 Modes of Reduced Current Consumption

4.2.1 Silent Mode

A falling edge at EN while TXD is high switches the IC into Silent mode. The TXD Signal has to be logic high during the Mode Select window (see Figure 4-2 on page 6). For EN and TXD either two independent outputs can be used, or two outputs from the same microcontroller port; in the second case, the mode change is only one command.

In Silent mode the transmission path is disabled. Supply current from V_{Batt} is typically I_{VSsi} = 40 µA with no load at the V_{CC} regulator.

The overall supply current from V_{Batt} is the result of 40 µA plus the V_{CC} regulator output current I_{VCCs}.

The 5V regulator is in low tolerance mode (4.65V to 5.35V) and can source up to 50 mA. In Silent mode the internal slave termination between pin LIN and pin VS is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present.

The Silent mode voltage is sufficient to run an external microcontroller on the ECU, for example in Power Down mode. The undervoltage reset is V_{CCthS} < 4.4V. If an undervoltage condition occurs, NRES is switched to low and the ATA6620N changes state to Pre-normal mode.

A falling edge at pin LIN followed by a dominant bus level maintained for a certain time period (t_{bus}) results in a remote wake-up request. The device switches from Silent mode to Pre-normal mode, then the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller and a high level at pin TXD (see Figure 4-3 on page 7).

With EN high, ATA6620N switches directly from Silent- via Pre-normal to Normal mode.

Figure 4-2. Switch to Silent Mode

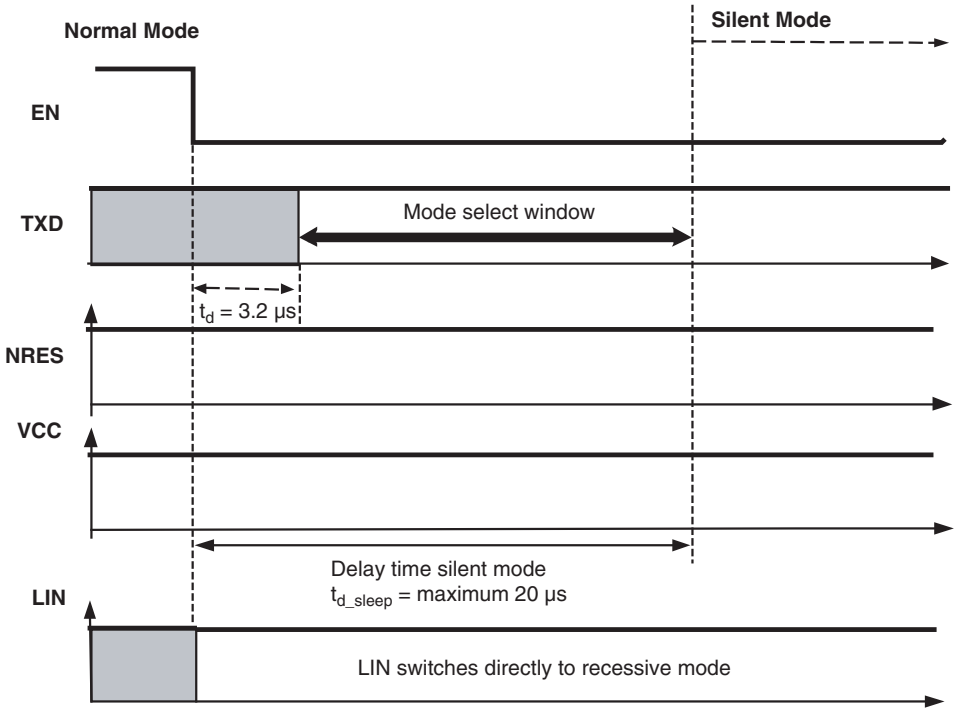
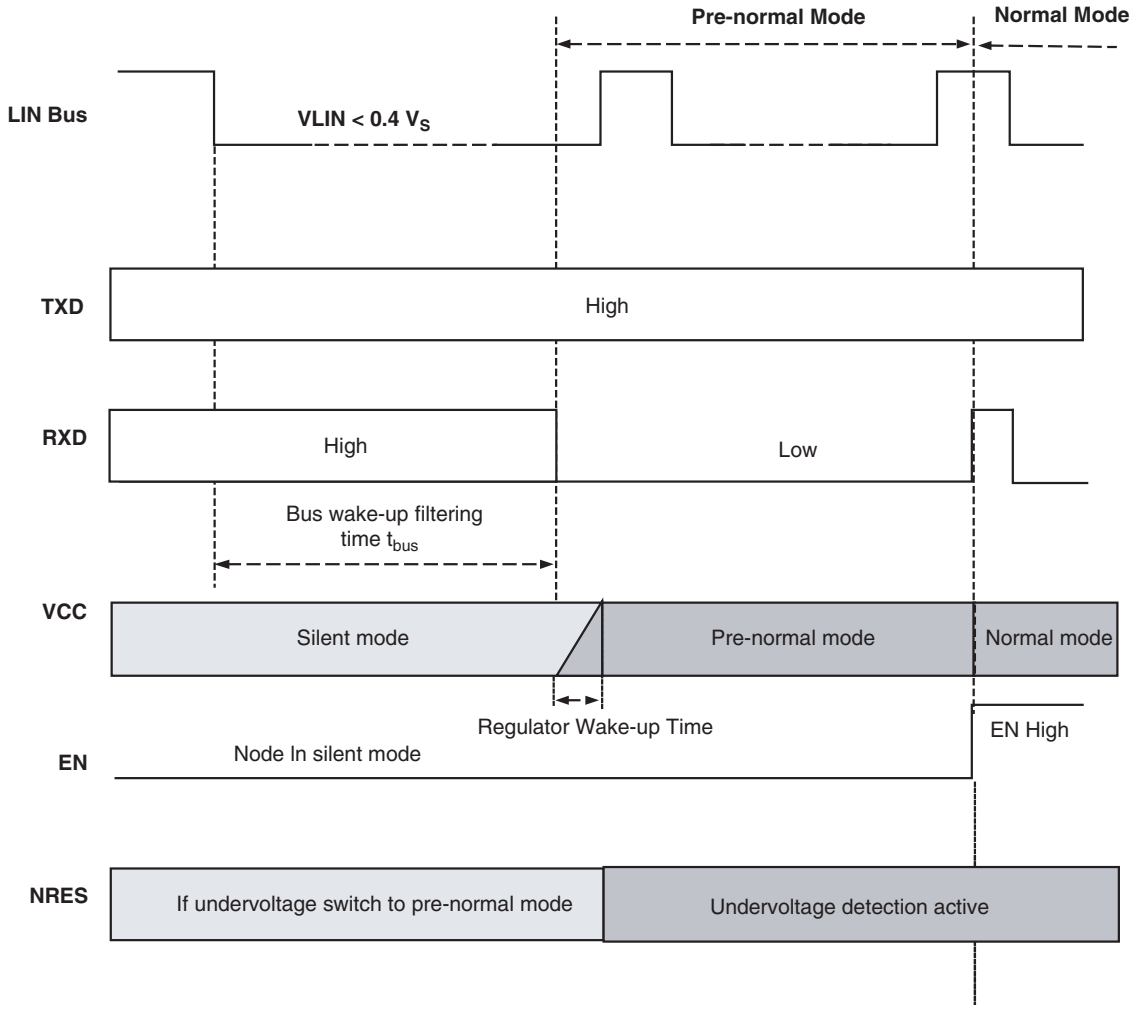


Figure 4-3. LIN Wake-up Waveform Diagram from Silent Mode



4.2.2 Sleep Mode

A falling edge at EN while TXD is low switches the IC into Sleep mode. The TXD Signal has to be logic low during the Mode Select window (see Figure 4-4). We recommend using the same microcontroller port for EN as for TXD; in this case the mode change is only one command.

In Sleep mode the transmission path is disabled. Supply current from V_{Batt} is typically $I_{VSsleep}$ = 10 µA. The V_{CC} regulator is switched off; NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present.

A falling edge at pin LIN followed by a dominant bus level maintained for a certain time period (t_{bus}) results in a remote wake-up request. The device switches from Sleep mode to Pre-normal mode. The V_{CC} regulator is activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller and a high level at pin TXD (see Figure 4-5 on page 9).

With EN high you can switch directly from Silent to Normal mode. In the application where the ATA6620N supplies the microcontroller, the wake-up from Sleep mode is only possible via pin LIN.

If the device is switched into Sleep mode, V_{CC} ramps down without generating an undervoltage reset at pin NRES.

Figure 4-4. Switch to Sleep Mode

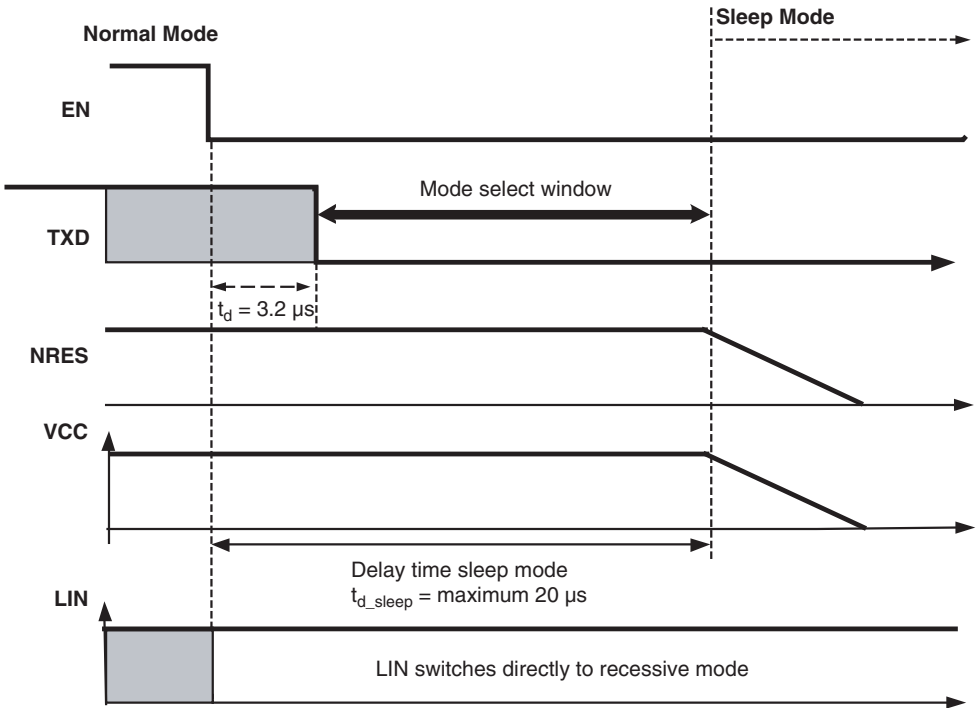
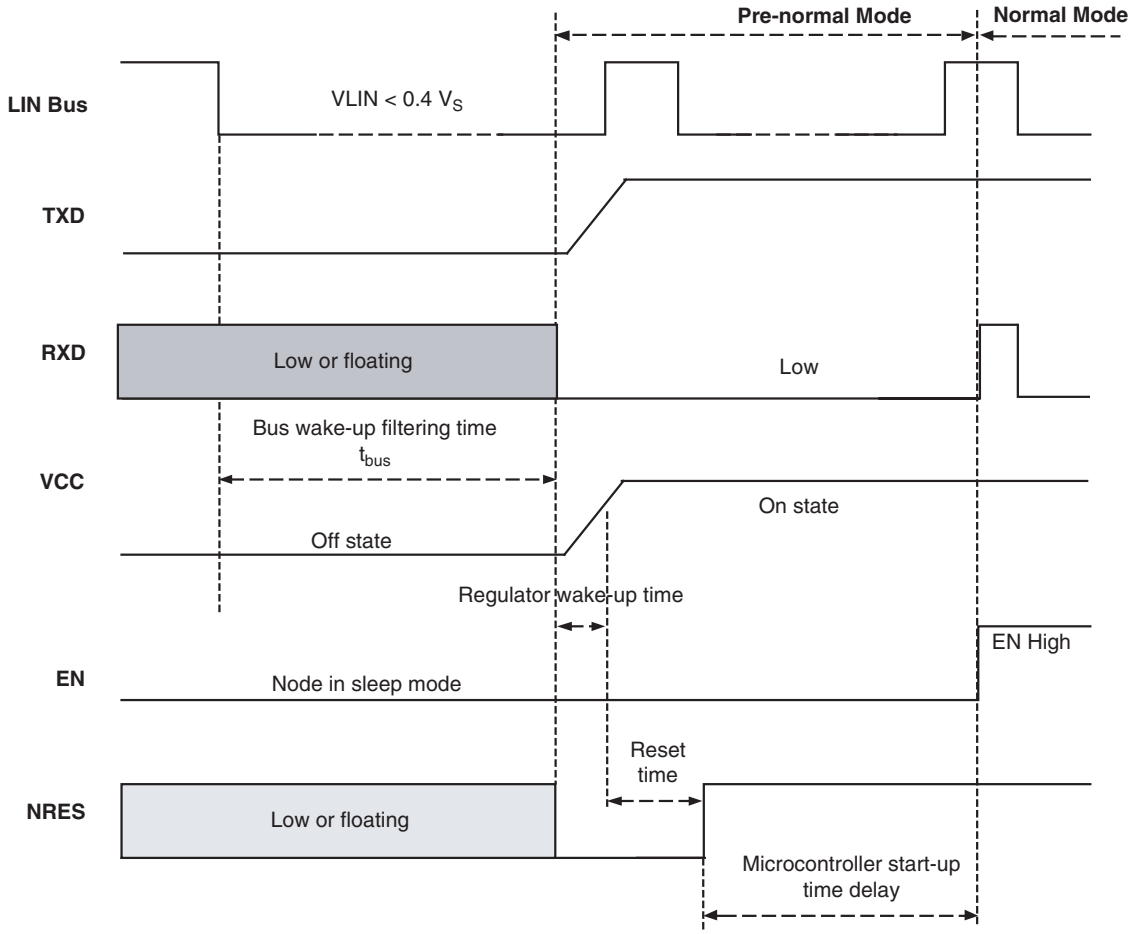


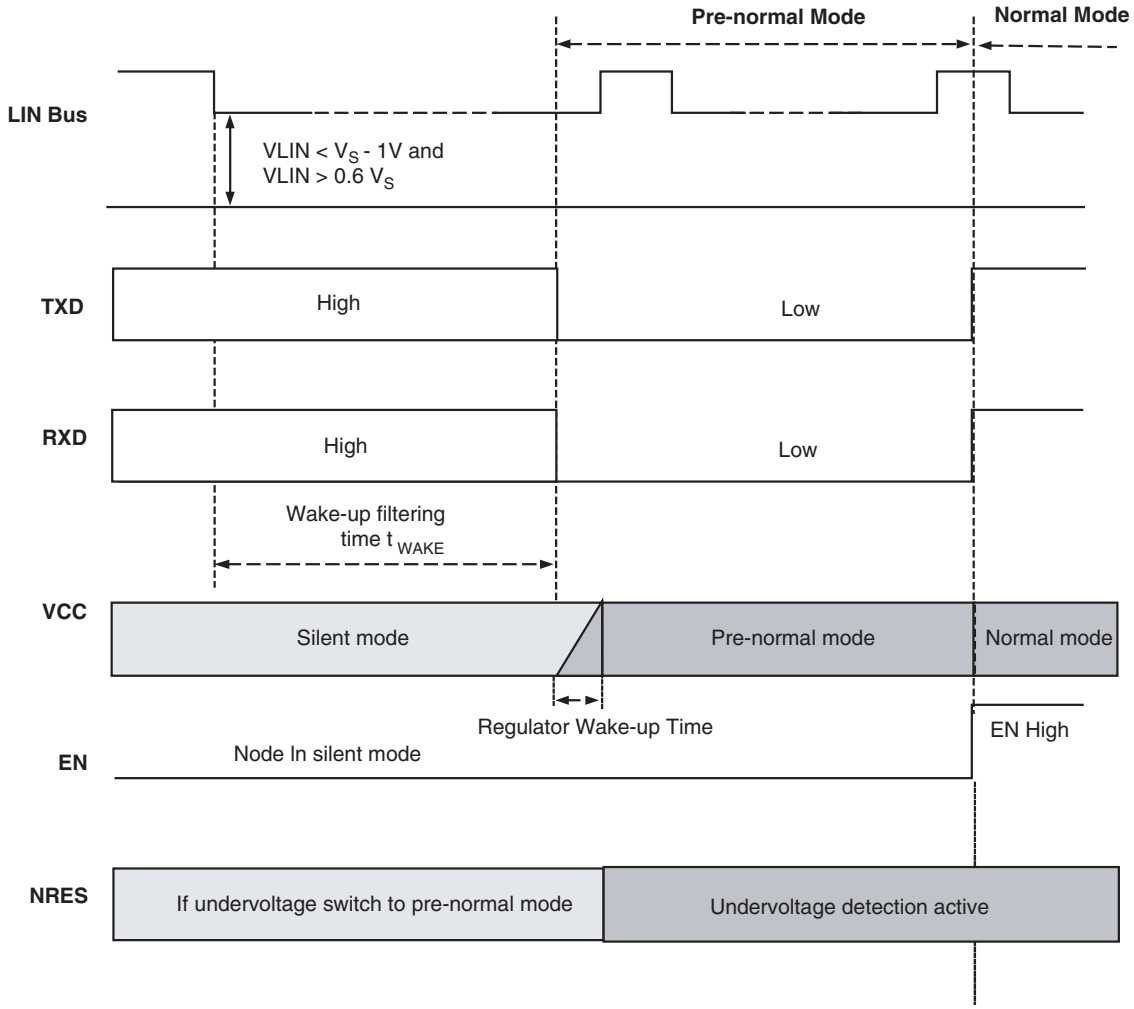
Figure 4-5. LIN Wake-up Diagram from Sleep Mode



4.2.3 Wake Up from Sleep/Silent Mode at an Insufficient Falling Edge at Pin LIN

If the ATA6620N is in Sleep mode or Silent mode and the voltage at the LIN Bus falls to a value lower than VLINL < V_S – 3.3V (see "Electrical Characteristics" numbers 9.5 and 9.6) but higher than 0.6 × V_S, then a wake up is detected and the circuit switches to pre-normal mode and the internal NMOS- transistor connected to the pin TXD is switched on and pulls down the pin TXD to Ground. The following figure shows the corresponding diagram for the wake-up from silent mode. The wake-up process from Sleep mode works analogue to this.

Figure 4-6. Wake Up from Silent Mode at an Insufficient Falling Edge at Pin LIN



When designing the complete system it has to be considered, that in this case (only in pre-normal mode) the pin TXD of the ATA6620N works as an output.

4.3 Pre-normal Mode

At system power-up the device automatically switches to Pre-normal mode. The voltage regulator is switched on (V_{CC} = 5V/50 mA) (see Figure 4-7 on page 11) after typically t_{VCC} > 300 µs. The NRES output switches to low for t_{res} = 10 ms and sends a reset to the microcontroller. LIN communication is switched off, and the undervoltage detection is active.

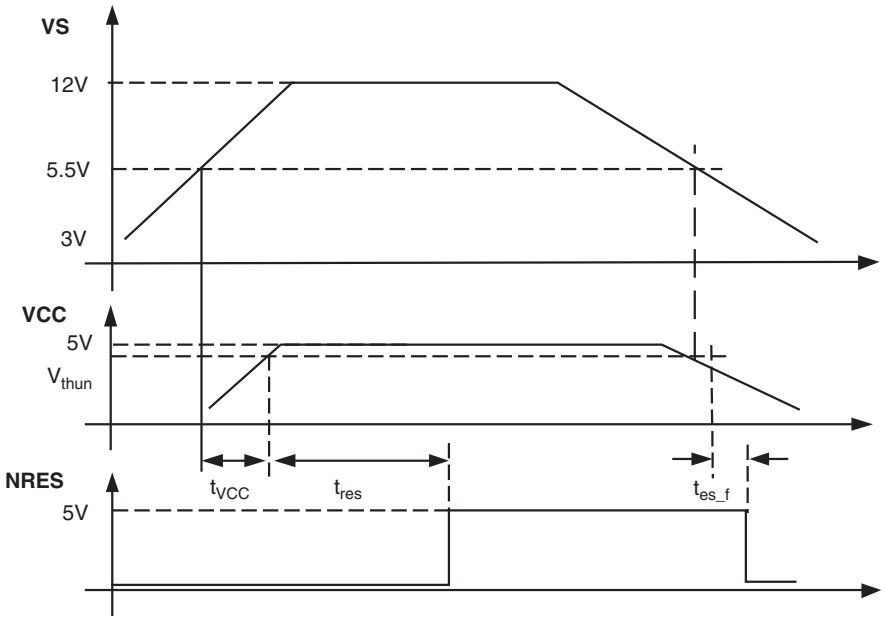
A power-down of V_{Batt} (V_S < 4.15V) during Silent or Sleep mode switches into Pre-normal mode after powering up the IC. During this mode the TXD pin is an output.

4.4 Unpowered Mode

If battery voltage is connected to the application circuit (see Figure 4-7), the voltage at the VS pin increases due to the block capacitor. When V_S is higher than the V_S undervoltage threshold, V_{Sth}, the IC-mode changes from Unpowered to Pre-normal mode. The V_{CC} output voltage reaches nominal value after t_{VCC}. This time depends on the V_{CC} capacitor and the load.

NRES is low for the reset time delay t_{Reset}; no mode change is possible during this time.

Figure 4-7. V_{CC} Voltage Regulator: Ramp Up and Undervoltage



5. Fail-safe Features

- During a short circuit at LIN, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds t_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of t_{hys}, switches the output on again. During LIN overtemperature switch-off, the V_{CC} regulator works independently.
- There are now reverse currents < 3 µA at pin LIN during loss of V_{Batt} or GND. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCCn}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into Pre–normal mode. If the chip temperature exceeds the value t_{VCCoff}, the V_{CC} output switches off. The chip cools down and after a hysteresis of t_{hys}, switches the output on again. Because of Pre-normal mode, the V_{CC} voltage will switch on again although EN is switched off from the microcontroller.The microcontroller can then start with normal operation.
- Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- Pin RXD is set floating if V_{Batt} is disconnected.
- Pin TXD provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.

6. Voltage Regulator

The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommend to use an tantalum capacitor with C > 10 µF and a ceramic capacitor with C = 100 nF. The values of these capacitors can be varied by the customer, depending on the application.

During mode change from Silent to Normal mode, the voltage regulator ramps up to 6V for only a few microseconds before it drops back to 5V. This behavior depends on the value of the load capacitor. With 4.7 µF, the overshoot voltage has its greatest value. This voltage decreases with higher or lower load capacitors.

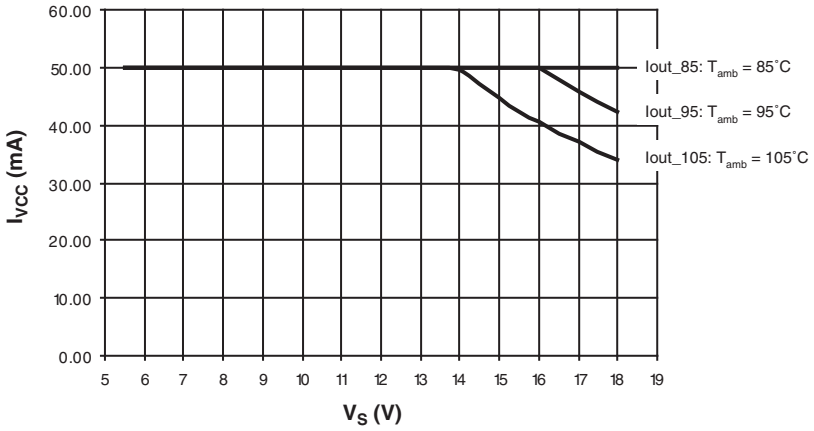
With this special SO8 package (fused lead frame to pin3) an R_{thja} of 80 K/W is achieved.

Therefore it is recommended to connect pin 3 with a wide GND plate on the printed board to get a good heat sink.

The main power dissipation of the IC is created from the V_{CC} output current I_{VCC}, which is needed for the application.

Figure 6-1 shows the safe operating area of the ATA6620N.

Figure 6-1. Save Operating Area versus V_{CC} Output Current and Supply Voltage V_S at Different Ambient Temperatures with R_{thja} = 80 K/W



For programming purposes of the microcontroller it is potentially necessary to supply the VCC output via an external power supply while the VS pin of the system basis chip is disconnected. This behavior is no problem for the system basis chip.

7. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500 ms T = 25°C Output current I_{VCC} ≤ 50 mA	V_S			+40	V
Pulse time ≤ 2 min T = 25°C Output current I_{VCC} ≤ 50 mA	V_S			27	V
Logic pins (RXD, TXD, EN, NRES)		–0.3		+6.5	V
Output current NRES	I_{NRES}	–2		+2	mA
LIN - DC voltage - Transient voltage		 –40 –150		 +60 +100	 V V
V_{CC} - DC voltage		 –0.3		 +6.5	 V
ESD (DIN EN 6100–4–2) Pin LIN, V_S versus GND according to LIN specification EMC Evaluation V 1.3		–6		+6	kV
HBM ESD S5.1 – all pins		–3		+3	kV
CDM ESD STM 5.3.1–1999 - All pins		 –1000		 +1000	 V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C
Operating ambient temperature	T_a	–40		+125	°C
Thermal resistance junction to ambient (free air)	R_{thja}			145	K/W
Special heat sink at GND (pin 3) on PCB	R_{thja}		80		K/W
Thermal shutdown of V_{CC} regulator	T_{VCCoff}	150	160	170	°C
Thermal shutdown of LIN output	T_{LINoff}	150	160	170	°C
Thermal shutdown hysteresis	T_{hys}		10		°C

8. Electrical Characteristics

5V < V_S < 18V, T_{amb} = –40°C to 125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**VS Pin**								
1.1	Nominal DC voltage range		VS	V_S	5	13.5	18	V	A
1.2	Supply current in Sleep mode	Sleep mode $V_{lin} > V_{Batt} – 0.5V$ $V_{Batt} < 14V$ (25°C to 125°C)	VS	$I_{VSsleep}$		10	20	µA	A
1.3	Supply current in Silent mode	Bus recessive; $V_{Batt} < 14V$ (25°C to 125°C) Without load at V_{CC}	VS	I_{VSsi}		40	50	µA	A
1.4	Supply current in Normal mode	Bus recessive Without load at V_{CC}	VS	I_{VSrec}			4	mA	A
1.5	Supply current in Normal mode	Bus dominant V_{CC} load current 50 mA	VS	I_{VSdom}			55	mA	A
1.6	Power On Reset threshold		VS	POR_{th}	3		3.3	V	D
1.7	Power On Reset threshold hysteresis		VS	POR_{hys}		0.1		V	D
1.8	V_S undervoltage threshold		VS	V_{Sth}	4.15	4.5	5	V	A
1.9	VS undervoltage threshold hysteresis		VS	V_{Sth_hys}		0.2		V	C
2	**RXD Output Pin**								
2.1	Low level input current	Normal mode; V_{LIN} = 0V V_{RXD} = 0.4V	RXD	I_{RXD}	2	5	8	mA	A
2.2	Low level output voltage	I_{RXD} = 1 mA	RXD	V_{RXDL}			0.3	V	A
2.3	Internal resistor to V_{CC}		RXD	R_{RXD}	3	5	7	kΩ	A
3	**TXD Input/Output Pin**								
3.1	Low level voltage input		TXD	V_{TXDL}	–0.3		+1.5	V	A
3.2	High level voltage input		TXD	V_{TXDH}	3.5		V_{CC} + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V	TXD	R_{TXD}	125	250	600	kΩ	A
3.4	High level leakage current	V_{TXD} = 5V	TXD	I_{TXD}	–3		+3	µA	A
3.5	Low-level output current	Pre-normal mode VTXD = 0.4V to 5V	TXD	$I_{TXDwake}$	2	5	8	mA	A
4	**EN Input Pin**								
4.1	Low level voltage input		EN	V_{ENL}	–0.3		+1.5	V	A
4.2	High level voltage input		EN	V_{ENH}	3.5		V_{CC} + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = 5V	EN	R_{EN}	125	250	600	kΩ	A
4.4	Low level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to 125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	**NRES Output Pin**								
5.1	High level output voltage	$V_S \geq 5.5V$; I_{NRES} = –1 mA	NRES	V_{NRESH}	4.5			V	A
5.2	Low level output voltage	$V_S \geq 5.5V$; I_{NRES} = +1 mA I_{NRES} = +250 µA	NRES	V_{NRESL} V_{NRESL}			0.2 0.14	V V	A A
5.3	Low level output low	10 kΩ to VCC; V_{CC} = 0.8V	NRES	V_{NRESLL}			0.2	V	A
5.4	Undervoltage reset time	$V_{VS} \geq 5.5V$ C_{NRES} = 20 pF	NRES	t_{Reset}	7		13	ms	A
5.5	Reset debounce time for falling edge	$V_{VS} \geq 5.5V$ C_{NRES} = 20 pF	NRES	t_{res_f}			3	µs	A
6	**Voltage Regulator VCC Pin in Normal and Pre-normal Mode**								
6.1	Output voltage V_{CC}	5.5V < V_S < 18V (0 mA – 50 mA)	VCC	V_{CCnor}	4.9		5.1	V	A
6.2	Output voltage V_{CC} at low V_S	3.3V < V_S < 5.5V	VCC	V_{CClow}	V_{VS} – V_D		5.1	V	A
6.3	Regulator drop voltage	V_S > 4.0V, I_{VCC} = –20 mA	VCC	V_D			250	mV	A
6.4	Regulator drop voltage	V_S > 4.0V, I_{VCC} = –50 mA	VCC	V_D			500	mV	A
6.5	Regulator drop voltage	V_S > 3.3V, I_{VCC} = –15 mA	VCC	V_D			200	mV	A
6.6	Output current	V_S > 3V	VCC	I_{VCC}	–50			mA	A
6.7	Output current limitation	V_S > 0V	VCC	I_{VCCs}	–200	–130		mA	A
6.8	Load capacity	1Ω < ESR < 5Ω at 100 kHz	VCC	C_{load}	1.8	2.2		µF	D
6.9	V_{CC} undervoltage threshold	Referred to V_{CC} V_S > 5.5V	VCC	V_{thunN}	4.4		4.8	V	A
6.10	Hysteresis of undervoltage threshold	Referred to V_{CC} V_S > 5.5V	VCC	$V_{hysthun}$	30			mV	A
6.11	Ramp up time V_S > 5.5V to V_{CC} > 4.9V	C_{VCC} = 4.7 µF No load	VCC	t_{VCC}			300	µs	A
7	**Voltage Regulator VCC Pin in Silent Mode**								
7.1	Output voltage V_{CC}	5.5V < V_S < 18V (0 mA – 50 mA)	VCC	V_{CCnor}	4.65		5.35	V	A
7.2	Output voltage V_{CC} at low V_S	3.3V < V_S < 5.5V (0 mA – 50 mA)	VCC	V_{CClow}	V_{VS} – V_D		5.1	V	A
7.3	Regulator drop voltage	V_S > 3.3V, I_{VCC} = 15 mA	VCC	V_D			200	mV	A
7.4	At V_{CC} undervoltage threshold the state switches back to Pre-normal mode	Referred to V_{CC} V_S > 5.5	VCC	V_{thunS}	3.9		4.4	V	A
7.5	Hysteresis of undervoltage threshold	Referred to V_{CC} V_S > 5.5V	VCC	$V_{hysthun}$	40			mV	D
7.6	Output current limitation	V_S > 0V	VCC	I_{VCCs}	–200	–130		mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to 125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8	**LIN Bus Driver: Bus Load Conditions: Load 1 (Small): 1 nF, 1 kΩ; Load 2 (Large): 10 nF, 500Ω; R_{RXD} = 5 kΩ; C_{RXD} = 20 pF 10.5, 10.6 and 10.7 Specifies the Timing Parameters for Proper Operation at 20 Kbps**								
8.1	Driver recessive output voltage	Load1/Load2	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500 Ω	LIN	$V_{_LoSUP}$			1.2	V	A
8.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500 Ω	LIN	$V_{_HiSUP}$			2	V	A
8.4	Driver dominant voltage	V_{VS} = 7V R_{load} = 1000 Ω	LIN	$V_{_LoSUP_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000 Ω	LIN	$V_{_HiSUP_1k}$	0.8			V	A
8.6	Pull–up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	60	kΩ	A
8.7	Self-adapting current limitation V_{BUS} = V_{Batt_max}	T_j = 125°C T_j = 27°C T_j = –40°C	LIN	I_{BUS_LIM}	52 100 120		110 170 230	mA mA mA	A
8.8	Input leakage current at the receiver including pull–up resistor as specified	Input Leakage current Driver off V_{BUS} = 0V V_{Batt} = 12V	LIN	$I_{BUS_PAS_dom}$	–1			mA	A
8.9	Leakage current LIN recessive	Driver off 8V < V_{Batt} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$	LIN	$I_{BUS_PAS_rec}$		15	20	µA	A
8.10	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND_{Device} = V_S V_{Batt} = 12V 0V < V_{BUS} < 18V	LIN	$I_{BUS_NO_gnd}$	–10	+0.5	+10	µA	A
8.11	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition	V_{Batt} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	I_{BUS}		0.5	3	µA	A
9	**LIN Bus Receiver**								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
9.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
9.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
9.4	Receiver input hysteresis	V_{hys} = V_{th_rec} – V_{th_dom}	LIN	V_{BUShys}	0.028 × V_S	0.1 × V_S	0.175 × V_S	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

8. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to 125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.5	Wake detection LIN High level input voltage		LIN	V_{LINH}	V_S – 1V		V_S + 0.3V	V	A
9.6	Wake detection LIN Low level input voltage	I_{LIN} = typically –3 mA	LIN	V_{LINL}	–27		V_S – 3.3V	V	A
10	**Internal Timers**								
10.1	Dominant time for wake–up via LIN bus	V_{LIN} = 0V		t_{bus}	30	90	150	µs	A
10.2	Time delay for mode change from Pre-normal into Normal mode via pin EN	V_{EN} = 5V		t_{norm}	5		20	µs	A
10.3	Time delay for mode change from Normal mode to Sleep mode via pin EN	V_{EN} = 0V		t_{sleep}	2	7	15	µs	A
10.4	TXD dominant time out timer	V_{TXD} = 0V		t_{dom}	6	10	20	ms	A
10.5	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S; $TH_{Dom(max)}$ = 0.581 × V_S; V_S = 7.0V to 18V; t_{Bit} = 50 ms D1 = $t_{bus_rec(min)}/(2 \times t_{Bit})$		D1	0.396				A
10.6	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_S; $TH_{Dom(min)}$ = 0.284 × V_S; V_S = 7.0V to 18V; t_{Bit} = 50ms D2 = $t_{bus_rec(max)}/(2 \times t_{Bit})$		D2			0.581		A
10.7	Slope time falling and rising edge at LIN			t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
10.8	Time delay for mode change from Silent- into Normal mode via EN	VEN = 5V		t_{s_n}	5	15	40	µs	A
11	**Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions (C_{RXD}): 20 pF; $R_{pull-up}$ = 2.4 kΩ**								
11.1	Propagation delay of receiver Switch to Sleep mode (see Figure 8-1 on page 18)	t_{rx_pd} = max(t_{rx_pdr}, t_{rx_pdf})		t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}		t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 8-1. Definition of Bus Timing Characteristics

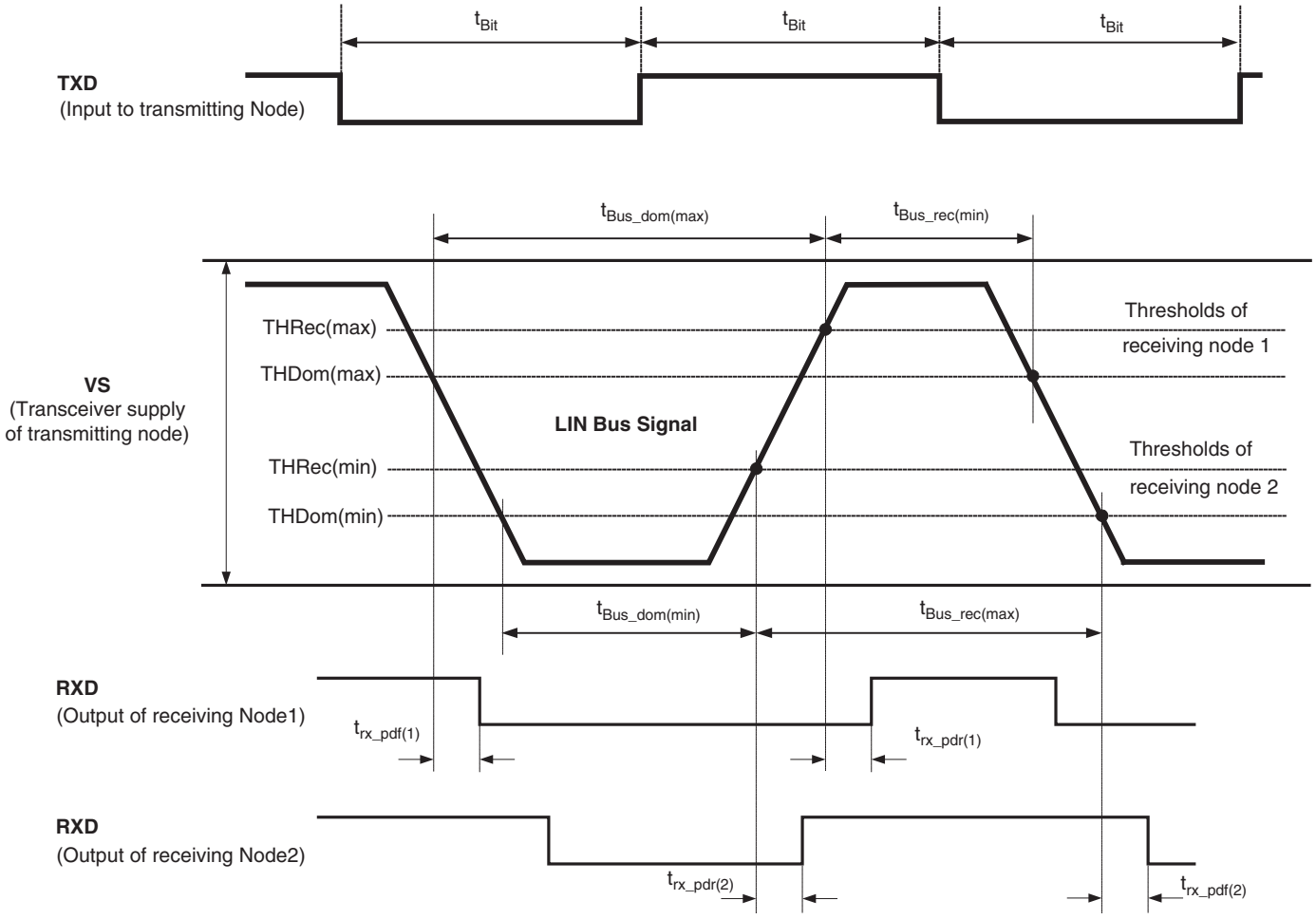
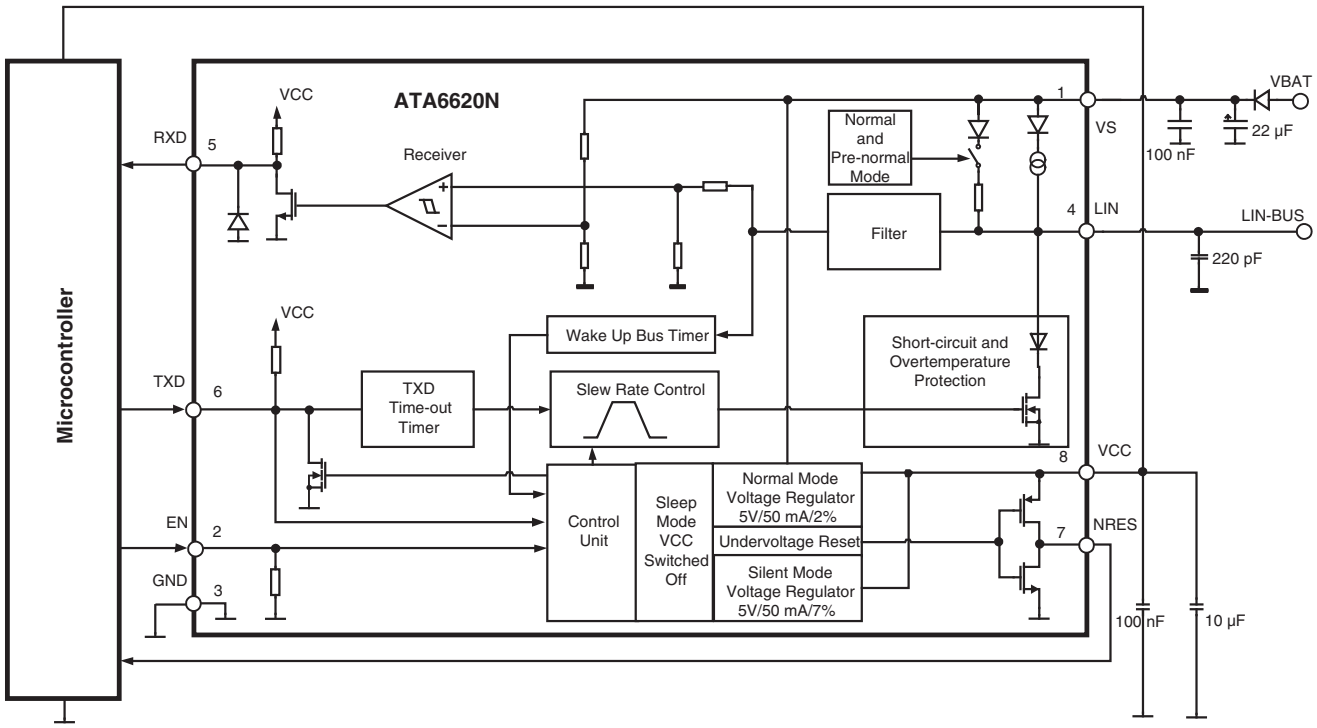


Figure 8-2. Application Circuit



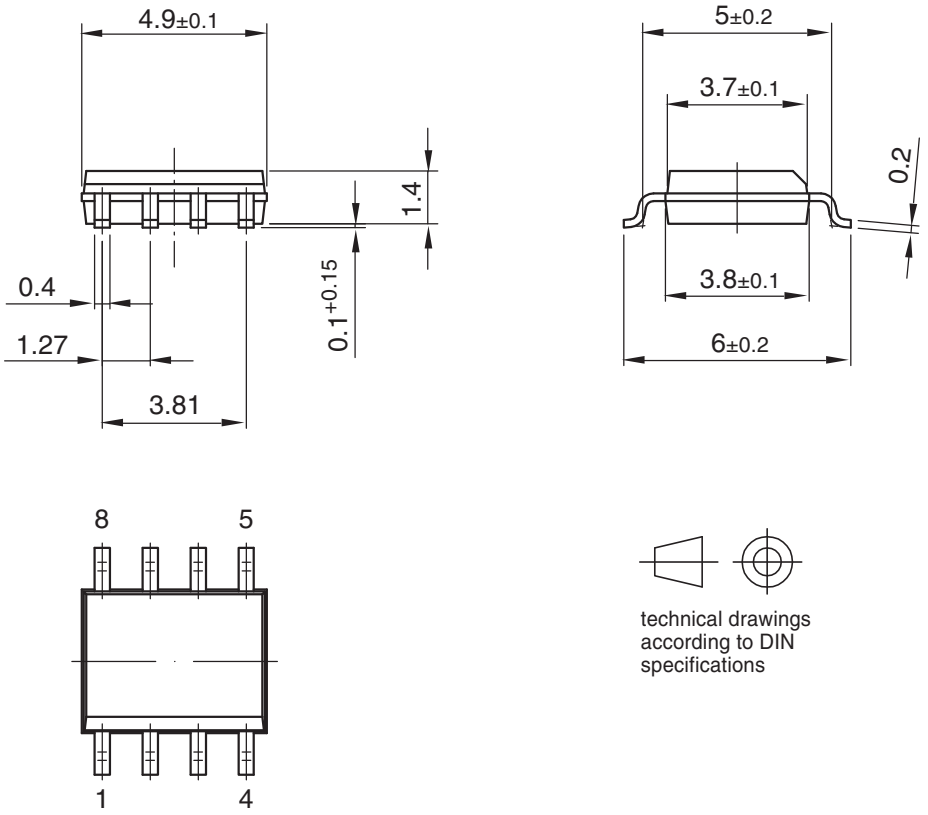
9. Ordering Information

Extended Type Number	Package	Remarks
ATA6620N-TAQY	SO8	LIN system basis chip, Pb-free, 4k, taped and reeled

10. Package Information

Package: SO 8

Dimensions in mm



Drawing-No.: 6.541-5031.01-4

Issue: 1; 15.08.06

11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4850I-AUTO-09/09	• Put datasheet in newest template • Heading 3.2: Supply Pin (VS): text changed • El. Characteristics table: row 1.9 changed
4850H-AUTO-12/07	• Section 3.1 “Physical Layer Compatibility” on page 3 added
4850G-AUTO-10/07	• Section 9 “Ordering Information” on page 20 changed
4850F-AUTO-07/07	• Put datasheet in a new template • Capital T for time generally changed in a lower case t • Section 3.4 “Undervoltage Reset Output (NRES) on page 3 changed • Section 4.2.2 “Sleep Mode” on page 8 changed • Section 6 “Voltage Regulator” on page 12 changed • Section 7 “Absolute Maximum Ratings” on page 13 changed • Section 8 “Electrical Characteristics” numbers 5.2, 5.3 and 6.8 on page 15 changed
4850E-AUTO-04/07	• Put datasheet in a new template • ATA6620 in ATA6620N renamed • Figure 1-1 “Block Diagram” on page 2 changed • Table 2-1 “Pin Description” on page 2 changed • Section 4-2 “Modes of Reduced Current Consumption” on page 6 changed • Figure 4-3 “LIN Wake-up Waveform Diagram from Silent Mode” on page 7 changed • Section 4.2.2 “Sleep Mode” on page 8 changed • Figure 4-5 “LIN Wake-up Diagram from Sleep Mode” changed • Section 4.2.3 “Wake-up from Sleep/Silent Mode at an Insufficient Falling Edge at pin LIN” on page 9 added • Section 4.3 “Pre-normal Mode” on page 10 changed • Section 8 “Electrical Characteristics” on pages 14 to 17 changed • Figure 8-2 “Application Circuit” on page 19 changed
4850D-AUTO-02/06	• Section 3.5 “Bus Pin (LIN)” on page 3 changed • Figure 4-1 “Mode of Operation” on page 4 changed • Figure 4-3 “LIN Wake-up Waveform Diagram from Silent Mode” on page 6 changed • Section 4.4 “Pre-normal Mode” on page 7 changed • Section 6 “Voltage Regulator” on page 10 changed • Figure 6-1 “Save Operating Area versus V_{CC} Output Current and Supply Voltage V_S at Different Ambient Temperatures” on page 10 changed • Table “Absolute Maximum Ratings” on page 11 changed • Table “Electrical Characteristics” from pages 12 to 15 changed

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